METHOD FOR MANUFACTURING A HIGH VOLTAGE MOSFET SEMICONDUCTOR DEVICE WITH ENHANCED CHARGE CONTROLLABILITY

ABSTRACT OF THE DISCLOSURE

A high voltage MOSFET device (100) has an nwell region (113) with a p-top layer (108) of opposite conductivity formed to enhance device characteristics. The p-top layer is implanted through a thin gate oxide, and is being diffused into the silicon later in the process using the source/drain anneal process. There is no field oxide grown on the top of the extended drain region, except two islands of field oxide close to the source and drain diffusion regions. This eliminates any possibility of p-top to be consumed by the field oxide, and allows to have a shallow p-top with very controlled and predictable p-top for achieving low on-resistance with maintaining desired breakdown voltage.